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EXAMINER	
THANGAVELU, KANDASAMY	

ART UNIT	PAPER NUMBER
2123	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/997,888	GOYAL ET AL.	
	Examiner	Art Unit	
	Kandasamy Thangavelu	2123	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 November 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *16-19* is/are allowed.

6)☒ Claim(s) *1-13* is/are rejected.

7)☒ Claim(s) *14 and 15* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *29 November 2001* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-19 of the application have been examined.

Drawings

2. The drawings submitted on November 23, 2001 are objected to: The figure number, title and the block identifiers are handwritten with non-uniform character sizes in Figure 5. Printed uniform character size is required.

Specification

3. The disclosure is objected to because of the following informalities:

Specification Page 10, Line 11, "delay output files and global clock con delay output file are merged" appears to be incorrect and it appears that it should be "delay output files and global clock cone delay output file are merged".

Appropriate correction is required.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains.

5. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

6. Claim 1 is rejected under 35 U.S.C. 103(a) as being unpatentable over **Boyle et al.** (U.S. Patent Application 2001/0010090) in view of **Ginetti** (U.S. Patent 6,622,291), and further in view of **Vanderweerd** (U.S. Patent Application 2004/0006584).

6.1 **Boyle et al.** teaches method for design optimization using logical and physical information. Specifically as per claim 1, **Boyle et al.** teaches a method for predicting delay of an ASIC design (Page 2, Para 0016, Item (c)), the method comprising the steps of:

(a) automatically partitioning a netlist into clusters (Page 1, Para 0008 and Para 0011; Page 2, Para 0016; Page 3, Para 0036 and 0037); and

(b) running respective instances of a delay prediction application (Page 2, Para 0016) on the clusters on at least two computers in parallel (Page 2, Para 0014; Page 3, Para 0038; Page 4, Para 0048; Page 5, Para 0049).

Boyle et al. does not expressly teach that the ASIC is a mufti-million gate sub-micron ASIC. **Ginetti** teaches that the ASIC is a mufti-million gate sub-micron ASIC (CL5, L59-61), because as per **Vanderweerd** present VLSI technology has integration density providing 8 million gates on a 100 mm^2 die (Page 1, Para 0009); and with deep sub-micron technologies, netlist optimization based on performance estimates are less accurate because the actual performance depends to a large extent on the detailed placement and routing (Page 2, Para 0013); and routing problems complicate the deep sub-micron ASIC design flow; with deep sub-micron technologies, the main source of delay is interconnection delay (Page 3, Para 0041 and 0045). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the method of **Boyle et al.** with the method of **Ginetti** that included the ASIC being a mufti-million gate sub-micron ASIC. The artisan would have been motivated because then present VLSI technology had integration density providing 8 million gates on a 100 mm^2 die; and with deep sub-micron technologies, netlist optimization based on performance estimates were less accurate because the actual performance depended to a large extent on the detailed placement and routing; and routing problems complicated the deep sub-micron ASIC design flow; with deep sub-micron technologies, the main source of delay was interconnection delay.

Boyle et al. does not expressly teach automatically partitioning a netlist into at least two logic cones. **Ginetti** teaches automatically partitioning a netlist into at least two logic cones (CL2, L42-44; CL2, L56-63; CL3, L11-17; Fig. 15-17), because they perform physical partitioning of the RTL cells into interconnected physical blocks (CL2, L42-44); the logic cones identify the timing arcs within each block enabling optimizing the timing arcs within each block

using the logic cones (CL3, L14-15); and provide a powerful and accurate timing model to model the timing behavior of the initial RTL description (CL3, L18-21); and the cones allow determination of critical arcs and non-critical arcs (CL17, L41-47). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the method of **Boyle et al.** with the method of **Ginetti** that included automatically partitioning a netlist into at least two logic cones. The artisan would have been motivated because they would perform physical partitioning of the RTL cells into interconnected physical blocks; the logic cones would identify the timing arcs within each block enabling optimizing the timing arcs within each block using the logic cones; and would provide a powerful and accurate timing model to model the timing behavior of the initial RTL description; and the cones would allow determination of critical arcs and non-critical arcs.

Boyle et al. teaches running respective instances of a delay prediction application (Page 2, Para 0016) on the clusters on at least two computers in parallel (Page 2, Para 0014; Page 3, Para 0038; Page 4, Para 0048; Page 5, Para 0049), because concurrent design optimization can be carried out in a parallel processing computer system (Page 3, Para 0035); parallel processing achieve high performance in design optimization (Page 2, Para 0019); as the clusters are loosely coupled, significant parallelism can be achieved by a parallel processing computer system (Page 3, Para 0038); and since logic optimization, routing and timing analysis operate on a few clusters at a time, each group involving a few clusters can be handled by a different independently executing thread and each thread can be executed in any CPU (Page 5, Para 0049). **Boyle et al.** does not expressly teach running respective instances of a delay prediction application on the logic cones on at least two computers in parallel. **Ginetti** teaches that automatically partitioning

a netlist into at least two logic cones (CL2, L42-44; CL2, L56-63; CL3, L11-17; Fig. 15-17), because they perform physical partitioning of the RTL cells into interconnected physical blocks (CL2, L42-44); the logic cones identify the timing arcs within each block enabling optimizing the timing arcs within each block using the logic cones (CL3, L14-15); and provide a powerful and accurate timing model to model the timing behavior of the initial RTL description (CL3, L18-21); and the cones allow determination of critical arcs and non-critical arcs (CL17, L41-47). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to combine the method of **Boyle et al.** involving running respective instances of a delay prediction application on the clusters on at least two computers in parallel with the method of **Ginetti** that included automatically partitioning a netlist into at least two logic cones. The artisan would have been motivated because they would perform physical partitioning of the RTL cells into interconnected physical blocks; the logic cones would identify the timing arcs within each block enabling optimizing the timing arcs within each block using the logic cones; and would provide a powerful and accurate timing model to model the timing behavior of the initial RTL description; and the cones would allow determination of critical arcs and non-critical arcs; and concurrent design optimization can be carried out in a parallel processing computer system; parallel processing achieve high performance in design optimization; as the clusters are loosely coupled, significant parallelism can be achieved by a parallel processing computer system; and since logic optimization, routing and timing analysis operate on a few clusters at a time, each group involving a few clusters can be handled by a different independently executing thread and each thread can be executed in any CPU.

7. Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over **Boyle et al.** (U.S. Patent Application 2001/0010090) in view of **Ginetti** (U.S. Patent 6,622,291) and **Vanderweerd** (U.S. Patent Application 2004/0006584), and further in view of **Dai et al.** (U.S. Patent Application 2003/0084416).

7.1 As per claim 2, **Boyle et al., Ginetti** and **Vanderweerd** teach the method of claim 1. **Boyle et al.** does not expressly teach partitioning the netlist into timing-independent cones of logic. **Ginetti** teaches that automatically partitioning a netlist into at least two logic cones (CL2, L42-44; CL2, L56-63; CL3, L11-17; Fig. 15-17), because they perform physical partitioning of the RTL cells into interconnected physical blocks (CL2, L42-44); the logic cones identify the timing arcs within each block enabling optimizing the timing arcs within each block using the logic cones (CL3, L14-15); and provide a powerful and accurate timing model to model the timing behavior of the initial RTL description (CL3, L18-21); and the cones allow determination of critical arcs and non-critical arcs (CL17, L41-47). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the method of **Boyle et al.** with the method of **Ginetti** that included automatically partitioning a netlist into at least two logic cones. The artisan would have been motivated because they would perform physical partitioning of the RTL cells into interconnected physical blocks; the logic cones would identify the timing arcs within each block enabling optimizing the timing arcs within each block using the logic cones; and would provide a powerful and accurate timing model to model the timing behavior of the initial RTL description; and the cones would allow determination of critical arcs and non-critical arcs.

Dai et al. teaches partitioning the netlist into timing-independent partitions and producing two or more netlists (Abstract, L16-22; Page 4, Para 0034, 0036 and 0039), because that enables each partition to independently satisfy the partition's spatial and timing constraints (Abstract, L16-22; Page 4, Para 0039). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to combine the method of **Boyle et al.** with the method of **Ginetti** that included automatically partitioning a netlist into at least two logic cones and the method of **Dai et al.** that included partitioning the netlist into timing-independent partitions and producing two or more netlists. The artisan would have been motivated because that would perform physical partitioning of the RTL cells into interconnected physical blocks; the logic cones would identify the timing arcs within each block enabling optimizing the timing arcs within each block using the logic cones; and would provide a powerful and accurate timing model to model the timing behavior of the initial RTL description; and the cones would allow determination of critical arcs and non-critical arcs; and that would enable each partition to independently satisfy the partition's spatial and timing constraints.

8. Claims 3-9 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Boyle et al.** (U.S. Patent Application 2001/0010090) in view of **Ginetti** (U.S. Patent 6,622,291) and **Vanderweerd** (U.S. Patent Application 2004/0006584), and further in view of **Dai et al.** (U.S. Patent Application 2003/0084416) and **Kapadia et al.** ("Using partitioning to help convergence in the standard-cell design automation methodology", ACM, June 1999).

8.1 As per claim 3, **Boyle et al., Ginetti, Vanderweerd** and **Dai et al.** teach the method of claim 2. **Boyle et al.** does not expressly teach partitioning the netlist into one global cone and multiple design cones. **Ginetti** teaches that automatically partitioning a netlist into at least two logic cones (CL2, L42-44; CL2, L56-63; CL3, L11-17; Fig. 15-17), because they perform physical partitioning of the RTL cells into interconnected physical blocks (CL2, L42-44); the logic cones identify the timing arcs within each block enabling optimizing the timing arcs within each block using the logic cones (CL3, L14-15); and provide a powerful and accurate timing model to model the timing behavior of the initial RTL description (CL3, L18-21); and the cones allow determination of critical arcs and non-critical arcs (CL17, L41-47). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the method of **Boyle et al.** with the method of **Ginetti** that included automatically partitioning a netlist into at least two logic cones. The artisan would have been motivated because they would perform physical partitioning of the RTL cells into interconnected physical blocks; the logic cones would identify the timing arcs within each block enabling optimizing the timing arcs within each block using the logic cones; and would provide a powerful and accurate timing model to model the timing behavior of the initial RTL description; and the cones would allow determination of critical arcs and non-critical arcs.

Kapadia et al. teaches partitioning the netlist into one global netlist and multiple design netlist (Page 593, CL1, Para 8 to CL2, Para 1; Page 593, CL2, Para 5 to Page 594, CL1, Para 1; Page 594, CL2, Para 5 to Page 595, CL1, Para 2), because that enables synthesis optimizations to be driven by accurate layout information (Page 593, CL1, Para5 to CL2, Para 1); and improves placement quality and reduces complexity (Page 593, CL2, Para 2); and decreases the

discrepancies in critical path timing between synthesis and layout (Page 594, CL1, Para 5). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to combine the method of **Boyle et al.** with the method of **Ginetti** that included automatically partitioning a netlist into at least two logic cones and the method of **Kapadia et al.** that included partitioning the netlist into one global netlist and multiple design netlist. The artisan would have been motivated because that would perform physical partitioning of the RTL cells into interconnected physical blocks; the logic cones would identify the timing arcs within each block enabling optimizing the timing arcs within each block using the logic cones; and would provide a powerful and accurate timing model to model the timing behavior of the initial RTL description; and the cones would allow determination of critical arcs and non-critical arcs; and that would enable synthesis optimizations to be driven by accurate layout information; and would improve placement quality and reduces complexity; and would decrease the discrepancies in critical path timing between synthesis and layout.

Per claim 4: **Boyle et al.** teaches merging output from the instances of the delay prediction application into a final output file (Fig. 2, SDF File). **Ginetti** also teaches merging output from the instances of the delay prediction application into a final output file (CL9, L8-10).

Per claim 5: **Boyle et al.** teaches using a partitioning program to automatically partition the netlist (Page 1, Para 0008 and Para 0011; Page 2, Para 0016; Page 3, Para 0036 and 0037).

8.2 As per claim 6, **Boyle et al., Ginetti, Vanderweerd, Dai et al.** and **Kapadia et al.** teach the method of claim 5. **Boyle et al.** does not expressly teach running the global clock cone through a monolithic delay prediction application. **Kapadia et al.** teaches running the global clock cone through a monolithic delay prediction application (Page 592, CL1, Para 1, Lines 16-19; Page 594, CL1, Para 2, L4-11), because that results in high correlation between synthesis estimates and post-placement measurements of wire-loads and gate delays (Page 592, CL1, Para 1, Lines 16-19). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to combine the method of **Boyle et al.** with the method of **Kapadia et al.** that included running the global clock cone through a monolithic delay prediction application. The artisan would have been motivated because that would result in high correlation between synthesis estimates and post-placement measurements of wire-loads and gate delays.

8.3 As per claim 7, **Boyle et al., Ginetti, Vanderweerd, Dai et al.** and **Kapadia et al.** teach the method of claim 6. **Boyle et al.** does not expressly teach inputting output from the monolithic delay prediction application and the design cones into the respective instances of delay prediction applications. **Kapadia et al.** teaches inputting output from the monolithic delay prediction application and the design cones into the respective instances of delay prediction applications (Page 593, CL2, Para 5 to Page 594, CL1, Para 3), because that results in high correlation between synthesis estimates and post-placement measurements of wire-loads and gate delays (Page 592, CL1, Para 1, Lines 16-19; Page 594, CL1, Para 5). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to combine the method of **Boyle et al.** with the method of **Kapadia et al.** that included inputting output from the

monolithic delay prediction application and the design cones into the respective instances of delay prediction applications. The artisan would have been motivated because that would result in high correlation between synthesis estimates and post-placement measurements of wire-loads and gate delays.

8.4 As per claim 8, **Boyle et al.** teaches a method for predicting delay of an ASIC design (Page 2, Para 0016, Item (c)), the method comprising the steps of:

(a) partitioning a netlist into clusters (Page 1, Para 0008 and Para 0011; Page 2, Para 0016; Page 3, Para 0036 and 0037);

(b) (c) performing delay calculation (Page 2, Para 0016) on the clusters in parallel (Page 2, Para 0014; Page 3, Para 0038; Page 4, Para 0048; Page 5, Para 0049); and

(d) merging results from the parallel delay calculations and the global delay calculation into an output file (Fig. 2, SDF File).

Boyle et al. does not expressly teach that the ASIC is a mufti-million gate sub-micron ASIC. **Ginetti** teaches that the ASIC is a mufti-million gate sub-micron ASIC (CL5, L59-61), because as per **Vanderweerd** present VLSI technology has integration density providing 8 million gates on a 100 mm^2 die (Page 1, Para 0009); and with deep sub-micron technologies, netlist optimization based on performance estimates are less accurate because the actual performance depends to a large extent on the detailed placement and routing (Page 2, Para 0013); and routing problems complicate the deep sub-micron ASIC design flow; with deep sub-micron technologies, the main source of delay is interconnection delay (Page 3, Para 0041 and 0045). It

would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the method of **Boyle et al.** with the method of **Ginetti** that included the ASIC being a mufti-million gate sub-micron ASIC. The artisan would have been motivated because then present VLSI technology had integration density providing 8 million gates on a 100 mm^2 die; and with deep sub-micron technologies, netlist optimization based on performance estimates were less accurate because the actual performance depended to a large extent on the detailed placement and routing; and routing problems complicated the deep sub-micron ASIC design flow; with deep sub-micron technologies, the main source of delay was interconnection delay.

Boyle et al. does not expressly teach partitioning a netlist into timing-independent cones including a global clock cone and multiple design cones. **Ginetti** teaches partitioning a netlist into multiple logic cones (CL2, L42-44; CL2, L56-63; CL3, L11-17; Fig. 15-17), because they perform physical partitioning of the RTL cells into interconnected physical blocks (CL2, L42-44); the logic cones identify the timing arcs within each block enabling optimizing the timing arcs within each block using the logic cones (CL3, L14-15); and provide a powerful and accurate timing model to model the timing behavior of the initial RTL description (CL3, L18-21); and the cones allow determination of critical arcs and non-critical arcs (CL17, L41-47). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the method of **Boyle et al.** with the method of **Ginetti** that included partitioning a netlist into multiple logic cones. The artisan would have been motivated because they would perform physical partitioning of the RTL cells into interconnected physical blocks; the logic cones would identify the timing arcs within each block enabling optimizing the timing arcs within each block using the logic cones; and would provide a powerful and accurate timing model to model the

timing behavior of the initial RTL description; and the cones would allow determination of critical arcs and non-critical arcs.

Dai et al. teaches partitioning the netlist into timing-independent partitions and producing two or more netlists (Abstract, L16-22; Page 4, Para 0034, 0036 and 0039), because that enables each partition to independently satisfy the partition's spatial and timing constraints (Abstract, L16-22; Page 4, Para 0039). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to combine the method of **Boyle et al.** with the method of **Ginetti** that included partitioning a netlist into multiple logic cones and the method of **Dai et al.** that included partitioning the netlist into timing-independent partitions and producing two or more netlists. The artisan would have been motivated because that would perform physical partitioning of the RTL cells into interconnected physical blocks; the logic cones would identify the timing arcs within each block enabling optimizing the timing arcs within each block using the logic cones; and would provide a powerful and accurate timing model to model the timing behavior of the initial RTL description; and the cones would allow determination of critical arcs and non-critical arcs; and that would enable each partition to independently satisfy the partition's spatial and timing constraints.

Kapadia et al. teaches partitioning the netlist into one global netlist and multiple design netlist (Page 593, CL1, Para 8 to CL2, Para 1; Page 593, CL2, Para 5 to Page 594, CL1, Para 1; Page 594, CL2, Para 5 to Page 595, CL1, Para 2), because that enables synthesis optimizations to be driven by accurate layout information (Page 593, CL1, Para5 to CL2, Para 1); and improves placement quality and reduces complexity (Page 593, CL2, Para 2); and decreases the discrepancies in critical path timing between synthesis and layout (Page 594, CL1, Para 5). It

would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to combine the method of **Boyle et al.** with the method of **Ginetti** that included partitioning a netlist into multiple logic cones and the method of **Kapadia et al.** that included partitioning the netlist into one global netlist and multiple design netlist. The artisan would have been motivated because that would perform physical partitioning of the RTL cells into interconnected physical blocks; the logic cones would identify the timing arcs within each block enabling optimizing the timing arcs within each block using the logic cones; and would provide a powerful and accurate timing model to model the timing behavior of the initial RTL description; and the cones would allow determination of critical arcs and non-critical arcs; and that would enable synthesis optimizations to be driven by accurate layout information; and would improve placement quality and reduces complexity; and would decrease the discrepancies in critical path timing between synthesis and layout.

Boyle et al. does not expressly teach performing delay calculation on the global clock cone. **Kapadia et al.** teaches performing delay calculation on the global clock cone (Page 592, CL1, Para 1, Lines 16-19; Page 594, CL1, Para 2, L4-11), because that results in high correlation between synthesis estimates and post-placement measurements of wire-loads and gate delays (Page 592, CL1, Para 1, Lines 16-19). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to combine the method of **Boyle et al.** with the method of **Kapadia et al.** that included performing delay calculation on the global clock cone. The artisan would have been motivated because that would result in high correlation between synthesis estimates and post-placement measurements of wire-loads and gate delays.

Boyle et al. does not expressly teach performing delay calculation on the multiple design cones using as input the delay calculation output of the global clock cone. **Kapadia et al.** teaches performing delay calculation on the multiple design nets using as input the delay calculation output of the global nets (Page 593, CL2, Para 5 to Page 594, CL1, Para 3), because that results in high correlation between synthesis estimates and post-placement measurements of wire-loads and gate delays (Page 592, CL1, Para 1, Lines 16-19; Page 594, CL1, Para 5). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to combine the method of **Boyle et al.** with the method of **Kapadia et al.** that included performing delay calculation on the multiple design nets using as input the delay calculation output of the global nets. The artisan would have been motivated because that would result in high correlation between synthesis estimates and post-placement measurements of wire-loads and gate delays.

Boyle et al. teaches performing delay calculation (Page 2, Para 0016) on the clusters on multiple computers in parallel (Page 2, Para 0014; Page 3, Para 0038; Page 4, Para 0048; Page 5, Para 0049), because concurrent design optimization can be carried out in a parallel processing computer system (Page 3, Para 0035); parallel processing achieve high performance in design optimization (Page 2, Para 0019); as the clusters are loosely coupled, significant parallelism can be achieved by a parallel processing computer system (Page 3, Para 0038); and since logic optimization, routing and timing analysis operate on a few clusters at a time, each group involving a few clusters can be handled by a different independently executing thread and each thread can be executed in any CPU (Page 5, Para 0049). **Boyle et al.** does not expressly teach performing delay calculation on the multiple design cones in parallel. **Ginetti** teaches that partitioning a netlist into multiple logic cones (CL2, L42-44; CL2, L56-63; CL3, L11-17; Fig.

15-17), because they perform physical partitioning of the RTL cells into interconnected physical blocks (CL2, L42-44); the logic cones identify the timing arcs within each block enabling optimizing the timing arcs within each block using the logic cones (CL3, L14-15); and provide a powerful and accurate timing model to model the timing behavior of the initial RTL description (CL3, L18-21); and the cones allow determination of critical arcs and non-critical arcs (CL17, L41-47). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to combine the method of **Boyle et al.** involving performing delay calculation on the clusters on multiple computers in parallel with the method of **Ginetti** that included partitioning a netlist into multiple logic cones. The artisan would have been motivated because they would perform physical partitioning of the RTL cells into interconnected physical blocks; the logic cones would identify the timing arcs within each block enabling optimizing the timing arcs within each block using the logic cones; and would provide a powerful and accurate timing model to model the timing behavior of the initial RTL description; and the cones would allow determination of critical arcs and non-critical arcs; and concurrent design optimization can be carried out in a parallel processing computer system; parallel processing achieve high performance in design optimization; as the clusters are loosely coupled, significant parallelism can be achieved by a parallel processing computer system; and since logic optimization, routing and timing analysis operate on a few clusters at a time, each group involving a few clusters can be handled by a different independently executing thread and each thread can be executed in any CPU.

8.5 As per claim 9, **Boyle et al., Ginetti, Vanderweerd, Dai et al.** and **Kapadia et al.** teach the method of claim 8. **Boyle et al.** does not expressly teach partitioning the netlist so that each of the multiple design cones includes approximately a same number of gates. **Ginetti** teaches partitioning a netlist into multiple logic cones (CL2, L42-44; CL2, L56-63; CL3, L11-17; Fig. 15-17), because they perform physical partitioning of the RTL cells into interconnected physical blocks (CL2, L42-44); the logic cones identify the timing arcs within each block enabling optimizing the timing arcs within each block using the logic cones (CL3, L14-15); and provide a powerful and accurate timing model to model the timing behavior of the initial RTL description (CL3, L18-21); and the cones allow determination of critical arcs and non-critical arcs (CL17, L41-47). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the method of **Boyle et al.** with the method of **Ginetti** that included partitioning a netlist into multiple logic cones. The artisan would have been motivated because they would perform physical partitioning of the RTL cells into interconnected physical blocks; the logic cones would identify the timing arcs within each block enabling optimizing the timing arcs within each block using the logic cones; and would provide a powerful and accurate timing model to model the timing behavior of the initial RTL description; and the cones would allow determination of critical arcs and non-critical arcs.

Kapadia et al. teaches partitioning the netlist so that each of the multiple local nets includes approximately a same number of gates (Page 594, CL1, Para 5; CL2, Para 1 and Para 4), because that results in low discrepancies in critical path timing between synthesis and layout (Page 594, CL1, Para 5). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to combine the method of **Boyle et al.** with the method of **Ginetti**

that included partitioning a netlist into multiple logic cones and with the method of **Kapadia et al.** that included partitioning the netlist so that each of the multiple design cones includes approximately a same number of gates. The artisan would have been motivated because they would perform physical partitioning of the RTL cells into interconnected physical blocks; the logic cones would identify the timing arcs within each block enabling optimizing the timing arcs within each block using the logic cones; and would provide a powerful and accurate timing model to model the timing behavior of the initial RTL description; and the cones would allow determination of critical arcs and non-critical arcs; and that would result low discrepancies in critical path timing between synthesis and layout.

9. Claims 10-13 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Boyle et al.** (U.S. Patent Application 2001/0010090) in view of **Ginetti** (U.S. Patent 6,622,291), **Vanderweerd** (U.S. Patent Application 2004/0006584), **Dai et al.** (U.S. Patent Application 2003/0084416) and **Kapadia et al.** ("Using partitioning to help convergence in the standard-cell design automation methodology", ACM, June 1999), and further in view of **Hahn et al.** (U.S. Patent 6,263,478) and **Kousai et al.** (U.S. Patent 2001/0015658).

9.1 As per claim 10, **Boyle et al., Ginetti, Vanderweerd, Dai et al.** and **Kapadia et al.** teach the method of claim 9. **Boyle et al.** does not expressly teach forming the global clock cone by identifying clock networks, reset pins, and logic controlled by a clock throughout the ASIC design. **Vanderweerd** teaches forming the global clock (Page 19, Para 0385; Page 20, Para 0386), because the global clock spans the complete system and act as the transfer clock to

facilitate communication between the local clocks (Page 20, Para 0386). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the method of **Boyle et al.** with the method of **Vanderweerd** that included forming the global clock. The artisan would have been motivated because the global clock would span the complete system and act as the transfer clock to facilitate communication between the local clocks.

Hahn et al. teaches identifying clock networks and reset pins (CL2, L63-67; CL3, L21-24; CL5, L20-30), because that allows performing timing analysis separately for the paths starting from each source clock edge, by tracing from the root of the clock distribution network (CL3, L21-24); and allows delay calculation to be performed on the clock network (Cl5, L28-30). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the method of **Boyle et al.** with the method of **Hahn et al.** that included identifying clock networks and reset pins. The artisan would have been motivated because that would allow performing timing analysis separately for the paths starting from each source clock edge, by tracing from the root of the clock distribution network; and delay calculation to be performed on the clock network.

Kousai et al. teaches identifying logic controlled by a clock throughout the ASIC design (Page 6, Para 0088), because that allows controlling the variations in the delay time of the clock signals (Page 6, Para 0088). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the method of **Boyle et al.** with the method of **Kousai et al.** that included identifying logic controlled by a clock throughout the ASIC design. The artisan would have been motivated because that would allow controlling the variations in the delay time of the clock signals.

9.2 As per claim 11, **Boyle et al., Ginetti, Vanderweerd, Dai et al., Kapadia et al., Hahn et al.** and **Kousai et al.** teach the method of claim 10. **Boyle et al.** does not expressly teach calculating delays for the global clock cone using a monolithic delay prediction application. **Kapadia et al.** teaches calculating delays for the global clock cone using a monolithic delay prediction application (Page 592, CL1, Para 1, Lines 16-19; Page 594, CL1, Para 2, L4-11), because that results in high correlation between synthesis estimates and post-placement measurements of wire-loads and gate delays (Page 592, CL1, Para 1, Lines 16-19). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to combine the method of **Boyle et al.** with the method of **Kapadia et al.** that included calculating delays for the global clock cone using a monolithic delay prediction application. The artisan would have been motivated because that would result in high correlation between synthesis estimates and post-placement measurements of wire-loads and gate delays.

11.3 As per claim 12, **Boyle et al., Ginetti, Vanderweerd, Dai et al., Kapadia et al., Hahn et al.** and **Kousai et al.** teach the method of claim 11. **Boyle et al.** does not expressly teach using a global delay output file and the design cones as input to parallel delay prediction applications. **Kapadia et al.** teaches using a global delay output file and the design cones as input to parallel delay prediction applications (Page 593, CL2, Para 5 to Page 594, CL1, Para 3), because that results in high correlation between synthesis estimates and post-placement measurements of wire-loads and gate delays (Page 592, CL1, Para 1, Lines 16-19; Page 594, CL1, Para 5). It would have been obvious to one of ordinary skill in the art at the time of

Applicants' invention to combine the method of **Boyle et al.** with the method of **Kapadia et al.** that included using a global delay output file and the design cones as input to parallel delay prediction applications. The artisan would have been motivated because that would result in high correlation between synthesis estimates and post-placement measurements of wire-loads and gate delays.

Per claim 13: **Boyle et al.** teaches allocating one computer to run one instance of the delay prediction application, and using each delay prediction application to perform delay calculations on one design cone (Page 2, Para 0016; Page 2, Para 0014; Page 3, Para 0038; Page 4, Para 0048; Page 5, Para 0049).

Allowable Subject Matter

10. Claims 14 and 15 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

11. Claims 16-19 are allowed.

Conclusion

12. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dr. Kandasamy Thangavelu whose telephone number is 571-272-3717. The examiner can normally be reached on Monday through Friday from 8:00 AM to 5:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kevin Teska, can be reached on 571-272-3716. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-305-9600.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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Art Unit 2123
March 4, 2005

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